UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/728,657	12/05/2003	Kam-Wing Li	4998P025	1273

8791 7590 07/27/2007

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

EXAMINER	
JUNTIMA, NITTAYA	

ART UNIT	PAPER NUMBER
2616	

MAIL DATE	DELIVERY MODE
07/27/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/728,657	LI, KAM-WING	
	Examiner	Art Unit	
	Nittaya Juntima	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12/5/03* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 2, 8-10, 13, 15, 20, and 25 are objected to because of the following informalities:

- in claim 2, line 6, "sampled" should be inserted before "number" to link the number of data values in the determining step to the number of data values in the sampling step;

- in claims 8 and 15, "is the" should be changed to "is a" to avoid lack of antecedent basis;

- in claim 9, line 2, a period is missing;

- in claim 10, line 1, "first" should be inserted before "timing" to refer to the timing signal associated with the first network protocol/VT 1.5 data stream and differentiate it from the second timing signal;

- in claim 13, line 10, "sampled" should be inserted before "phase difference signal" to link the sampling of the phase difference signal in line 9 to a generation of a phase metric signal in line 10;

- in claim 20, line 12, "sampled" should be inserted before "phase difference signal" to link the sampling of the phase difference signal in line 11 to a generation of a phase metric signal in line 12;

- in claim 25, line 6, "sampled" should be inserted before "number" to link the number of data values in means for determining a phase metric to means for sampling.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-11, 13-19, and 24-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Choi (US 5,131,013).

Regarding claim 1, as shown in Fig. 5, Choi teaches a method comprising:

Extracting data (VT payload) from a data stream (VT-G signal) formatted according to a first network protocol (SONET). See col. 6, lines 9-31 and claims 13 and 16.

Storing the extracted data in a buffer (synchronizing elastic store 202) based on a first timing signal (synchronous timing signal, i.e., the write clock signal) associated with the data stream (col. 6, lines 15-20, 28-31, col. 3, lines 49-53).

Reading the extracted data from the buffer (synchronizing elastic store 202) based on a second timing signal (the read clock signal) associated with a second network protocol (asynchronous digital signal). See col. 7, lines 5-10, 20-22, and claim 13.

Generating stuff bits for a data stream (DS1 digital signal) according to the second network protocol (asynchronous digital signal) based on a phase difference (a phase difference represented by a write-read separation signal generated by a phase detector 203) between the first timing signal (the write clock signal) and the second timing signal (the read clock signal). See col. 6, lines 53-67, col. 3, lines 55-col. 4, lines 18, col. 7, lines 5-26, see also col. 2, lines 62-68 and claim 16.

Regarding claim 2, Choi also teaches:

Sampling a number of data values stored in the buffer (a number of data values stored in the synchronizing elastic store 202,Fig. 5 is represented by a write-read address separation/phase difference signal) based on the first timing signal (the write clock signal) (low pass filter 205 contains a sampler 206,Fig. 3 that samples the raw write-read address separation signal output from phase detector 203 to smooth the effects of the phase jumps in the write-read address separation signal caused by the gaps in the write clock signal, col. 7, lines 10-20, see also col. 6, lines 62-67 and col. 3, lines 67-col. 4, lines 29 and claim 11).

Determining a phase metric (stuff control signal generated by low pass filter 207, Fig. 5) based on the sampled number of data values stored in the buffer (the sampled write-read address separation/phase difference signal). See col. 7, lines 16-20, see also col. 6, lines 62-67 and col. 4, lines 8-43.

Determining a rate (a stuff rate) at which stuff bits are to be inserted in a data stream according to the second network protocol (asynchronous digital signal) based on the phase metric (stuff control signal generated by low pass filter 207, Fig. 5). A stuff decision generated by a ¼ DS2 mapping and stuffing control 509,Fig.5 to control the read clock must comprise stuff rate, see col. 7, lines 16-20, see also col. 6, lines 62-67 and col. 4, lines 12-18.

Regarding claim 3, Choi teaches that the phase metric (stuff control signal generated by low pass filter 207, Fig. 5) comprises an average number of data values stored in the buffer (an average sampled write-read address separation/phase difference signal) using a moving average filter, see col. 6, lines 62-67 and col. 4, lines 40-55.

Regarding claim 4, Choi also teaches that the second network protocol comprises a plesiochronous network protocol (asynchronous digital signal). See col. 6, lines 52-60 and claims 13 and 16.

Regarding claim 5, Choi also teaches formatting the extracted data and the stuff bits as a data stream (a DS1 digital signal) according to the second network protocol (asynchronous digital signal) (the read data signal from the elastic store 202,Fig. 5 is mapped into DS1 digital signal by unit 509, col. 6, lines 52-60, col. 7, lines 20-22, and claims 13 and 16).

Regarding claim 6, Choi teaches that the data stream according to the second network protocol comprises a DS 1 data stream (col. 6, lines 52-60, col. 7, lines 20-22, and claims 13 and 16).

Regarding claims 7 and 8, Choi also teaches that the first network protocol comprises a synchronous network/SONET protocol (col. 6, lines 52-60 and claims 13 and 16).

Regarding claim 9, Choi also teaches that the data stream formatted according to the first network protocol comprises a VT1.5 formatted data stream (col. 6, lines 52-60 and claim 16).

Regarding claim 10, Choi also teaches that the first timing signal comprises a clock signal for the VT1.5 formatted data stream (col. 6, lines 28-31 and 52-60).

Regarding claim 11, it is inherent that the first timing signal (synchronous timing signal, i.e., the write clock signal = VT1.5 clock signal rate of 1.728 Mb/s and VT1.5 frame signal of 8 KHz, col. 5, lines 32-33) and the second timing signal (asynchronous timing signal, i.e., the read clock signal = DS1 clock signal rate of 1.544 Mb/s and frame signal of 8 KHz, col. 6, lines 52-60 and claims 14 and 16) have approximately the same average frequency.

Claims 13-19 are apparatus claims corresponding to method claims 2, 3, 8, 9, 4, 6, and 11, respectively, and are therefore rejected under the same reason set forth in the rejection of claims 2, 3, 8, 9, 4, 6, and 11, respectively (in claim 13, a buffer reads on elastic store 202, a phase detector reads on phase detector 203, a filter reads on filer 205 containing sampler 206, and a stuff rate generator reads on a ¼ DS2 mapping and stuff control 509 in Fig. 5).

Claims 24-26 are apparatus claims corresponding to method claims 1, 2, and 5, respectively and are therefore rejected under the same reason set forth in the rejection of claims 1, 2, 5, respectively.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Choi (US 5,131,013) in view of Bleisteiner (US 2002/0191724 A1).

Regarding claim 12, Choi does not explicitly teach that the buffer (the elastic store 202, Fig. 5) comprises a FIFO queue. However, as shown in Fig. 2, Bleisteiner teaches that an elastic store 14 is a FIFO register (paragraph 15, see also Fig. 4 and paragraph 21). Therefore, it would have been obvious to one skilled in the art to include a FIFO register such that the buffer would comprise a FIFO queue as claimed. The suggestion/motivation to do so would have been to implementing the buffer using register or the like as suggested by Choi (col. 3, lines 26-29) so that data can be written into and read out in a first-in, first-out fashion.

6. Claims 20-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Choi (US 5,131,013) in view of Tanis (US 2004/0120360 A1).

Regarding claim 20, as shown in Fig. 5, Choi teaches a system comprising a buffer (elastic store 202), a phase detector (a phase detector 203), a filter (filer 205 containing sampler 206), and a stuff rate generator (a ¼ DS2 mapping and stuff control 509) that perform functions as recited in method claim 2, and are therefore rejected under the same reason set forth in the rejection of claim 2 with an exception that Choi does not teach a switch fabric and that the data stream (VT-G signal) is received from the switch fabric as recited in the claim.

However, as shown in Fig. 1, Tanis teaches a switch fabric (40) that outputs a SDF frame, which is a modified version of a SONET STS-1 frame containing modified version of VTs, into an output side interface 70C DS3 in an outbound direction (paragraphs 4 and 18-20).

Given the teaching of Tanis, it would have been obvious to one skilled in the art at the time of the invention was made to further modify the teaching of Choi such that a switch fabric would be included and the data stream (VT signal on modified STS1/SDF frame) would be received from the switch fabric as claimed. The suggestion/motivation to do so would have been to enable the outputs from switch fabric to be converted into format originally received at the input to the input side interface of the switch fabric (Tanis, paragraph 19).

Claims 21-23 contain limitationd similar to method claims 2, 9, and 6, respectively, and are therefore, rejected under the same reason set forth in the rejection of claims 2, 9, and 9, respectively.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- US 7,227,876 B1 disclosing buffer dept estimator for asynchronous gapped signal (whole);

- US 5,337,334 disclosing synchronous digital signal to asynchronous digital signal desynchronizer (Abstract and Figs. 1-2).

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nittaya Juntima whose telephone number is 571-272-3120. The examiner can normally be reached on Monday through Friday, 8:00 A.M - 5:00 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on 571-272-3155. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Nittaya Juntima
Patent Examiner, AU 2616
July 20, 2007